REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-6 and 14-17 are pending in the present application. Claim 1 is amended and new Claims 15-17 are added by the present amendment.

In the outstanding Office Action, Claims 1-3 and 14 were rejected under 35 U.S.C. § 102(a or e) as anticipated by Asao et al. (U.S. Patent No. 6,590,244, herein "Asao"); Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as unpatentable over Asao in view of Pan et al. (U.S. Patent No. 6,548, 849, herein "Pan"); and Claim 6 was rejected under 35 U.S.C. § 103(a) as unpatentable over Asao in view of Scheuerlein et al., IEEE International Solid State Circuits Conference.

Regarding the rejection of Claims 1-3 and 14 under 35 U.S.C. § 102(a or e) as anticipated by Asao, independent Claim 1 has been amended to recite that a magnetic layer provided between a third wiring line and a fourth wiring line is separated from both of the third wiring line and the fourth wiring line and the magnetic layer is electrically connected to only one of the third wiring line and the fourth wiring line via a nonmagnetic layer. The claim amendments find support in Figure 11 and its corresponding description in the specification. No new matter has been added.

Briefly recapitulating, amended Claim 1 is directed to a magnetic memory device that has a memory cell and a peripheral circuit. The peripheral circuit includes a third wiring line and a fourth wiring line and a magnetic layer provided between the third wiring line and the fourth wiring line. The magnetic layer is separated from both of the third wiring line and the fourth wiring line, and the magnetic layer is electrically connected to only one of the third wiring line and the fourth wiring line via a nonmagnetic layer.

In a non-limiting example, Figure 11 shows the peripheral circuit (core peripheral circuit) having the third wiring line 20c, the fourth wiring line 21c, the magnetic layer 116_{-3}, and the nonmagnetic layer 116_{-2}.

The claimed magnetic memory device advantageously suppresses, when bit lines and write word lines are arranged closer to one another to decrease a write current, inductance components generated due to the proximity of the wiring lines, by utilizing a magnetic layer (magnetic material) and a nonmagnetic layer that form a TMR (Tunneling Magneto Resistive) element.

More specifically, the magnetic memory device of Claim 1 is configured to provide, in an MRAM having a memory cell and a core peripheral circuit, an MTJ film 27a composed of a tunnel junction layer (nonmagnetic layer) 116_{-2} and a magnetic recording layer (memory layer) 116_{-3} on a wiring line 20c in the fourth level of a core peripheral circuit. The wiring line 20c in the fourth level and a wiring line 21c in the fifth level are not electrically connected, as shown for example in Figure 11.

Thereby, even when the bit line 21a and the write word lines 19b and 19d are arranged close from each other, the device of Claim 1 is capable of suppressing the generation of an electromotive force between wiring lines 19f and 21c that are brought closer to each other. Thus, the interference caused by the electromotive force between the wiring lines 19f and 21c can be reduced.

Further, the memory device of Claim 1 by adopting a structure in which the magnetic recording layer 116_{-3} is arranged on the wiring line 20c in the fourth level via the tunnel junction layer 116_{-2}, it is possible to reliably perform, for example, a CMP (Chemical Mechanical Polishing) processing for planarizing an insulator film 16, without degeneration in cost performance. It is also possible to use the wiring line 20c in the fourth level and the wiring line 21c in the fifth level provided above and below the magnetic recording layer 116_{-3}

as separate wiring lines, and thereby an advantage of increased flexibility in design is obtained by the structure of Claim 1.

As discussed above, the structure of the magnetic memory of Claim 1 in which one end of the tunnel junction layer 116_{-2} is connected to the magnetic recording layer 116_{-3} and the other end is connected to the wiring line 20c in the fourth level is not disclosed in any of the applied art. With this claimed structure, it is possible not only to suppress a parasitic inductance in a core peripheral circuit, but also to utilize the wiring line 20c in the fourth level and the wiring line 21c in the fifth level as separate wiring lines. These effects obtained from the above-described structure cannot be obtained from any of the applied art.

Turning to the applied art, Asao shows in Figure 1 a semiconductor memory device having a third wiring line 19b, a fourth wiring line 20b, magnetic elements 41 and 43, and a nonmagnetic layer 42. However, Asao does not teach or suggest that the magnetic layers 41 and 43 are provided between the third and fourth wiring lines such that the magnetic layers 41 and 43 are separated from both the third and fourth wiring lines 19b and 20b and the magnetic layers electrically connect only one of the third and fourth wiring lines via a nonmagnetic layer as requested by amended Claim 1.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom patentably distinguish over Asao.

New Claims 15-17 have been added to set forth the invention in a varying scope and Applicants submit the new claims are supported by the originally filed specification. New Claims 15-17 depend from independent Claim 1, which is believed to be allowable as noted above. Accordingly, it is respectfully submitted new Claims 15-17 are allowable for similar reasons as discussed above.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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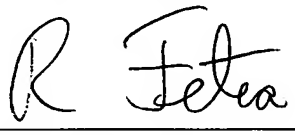

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